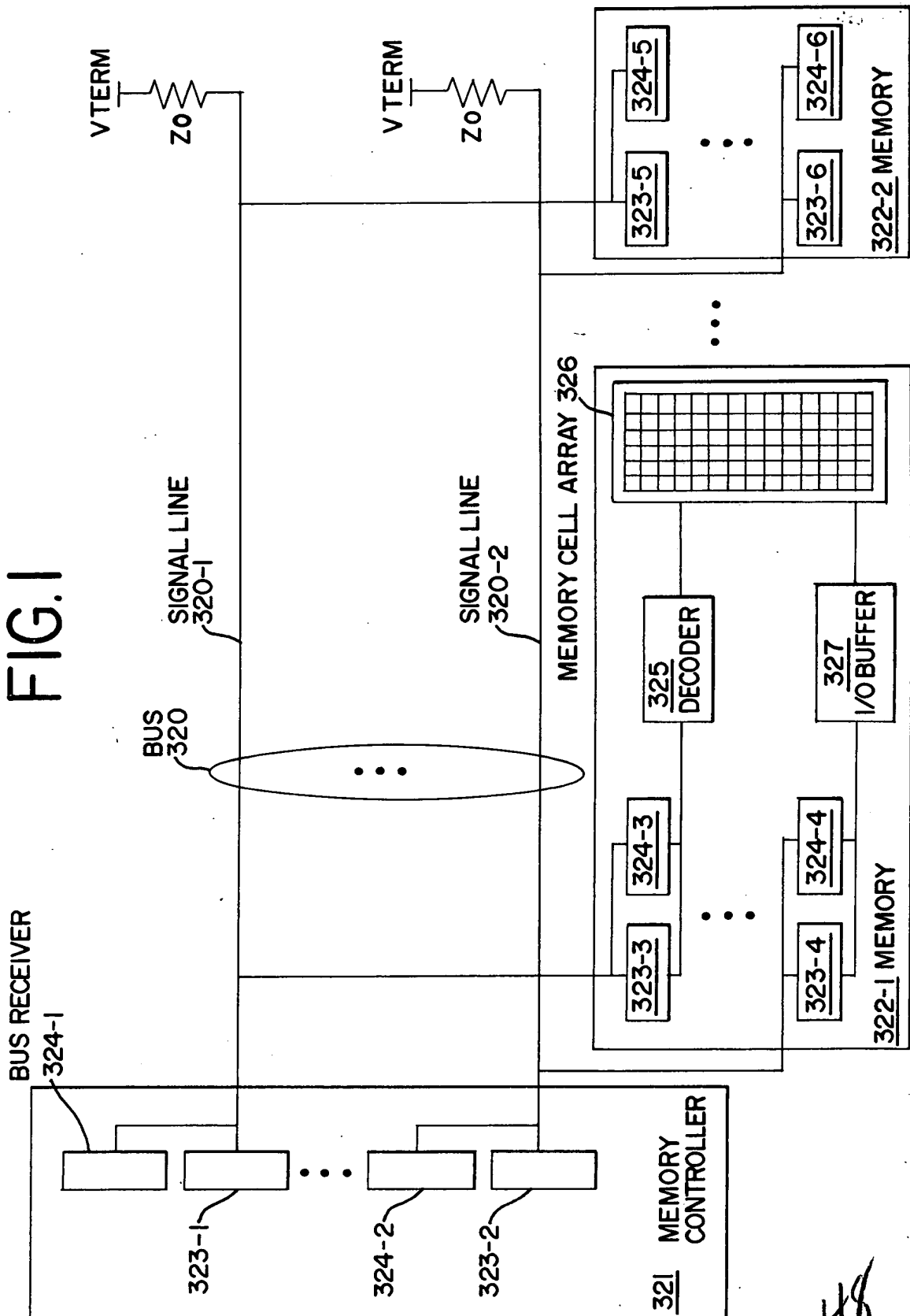


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FIG.2

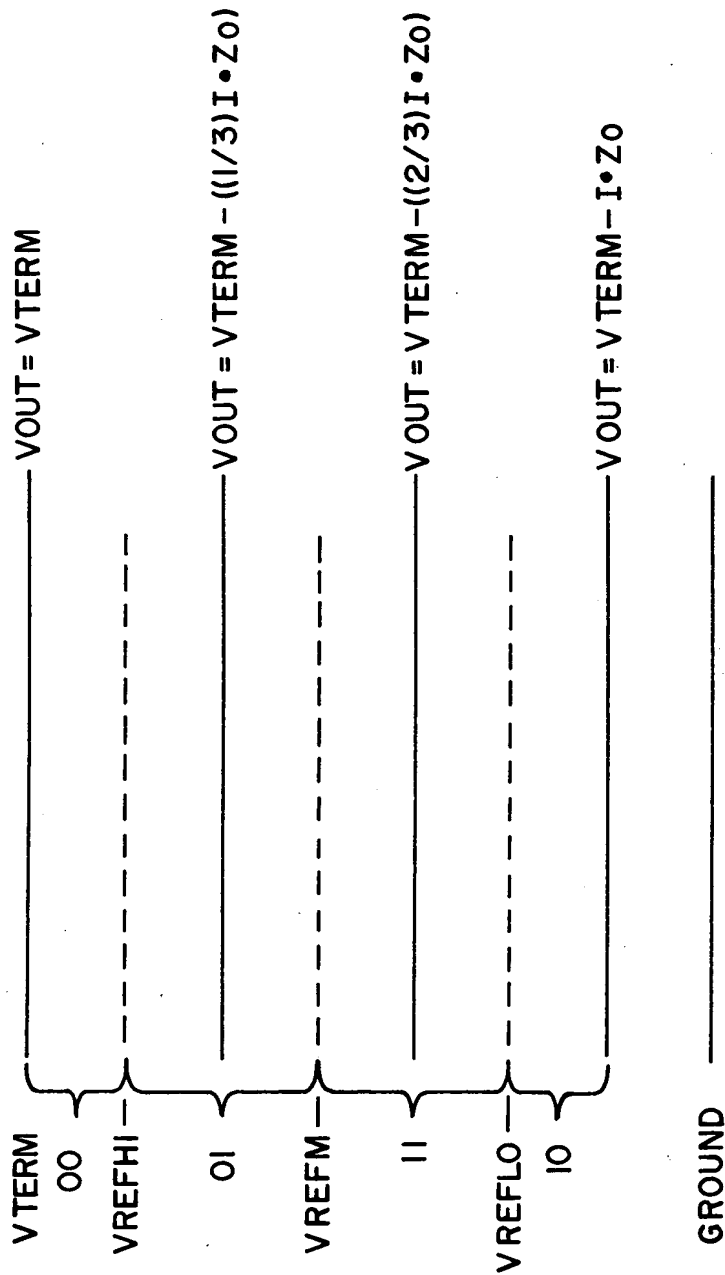


FIG. 3A

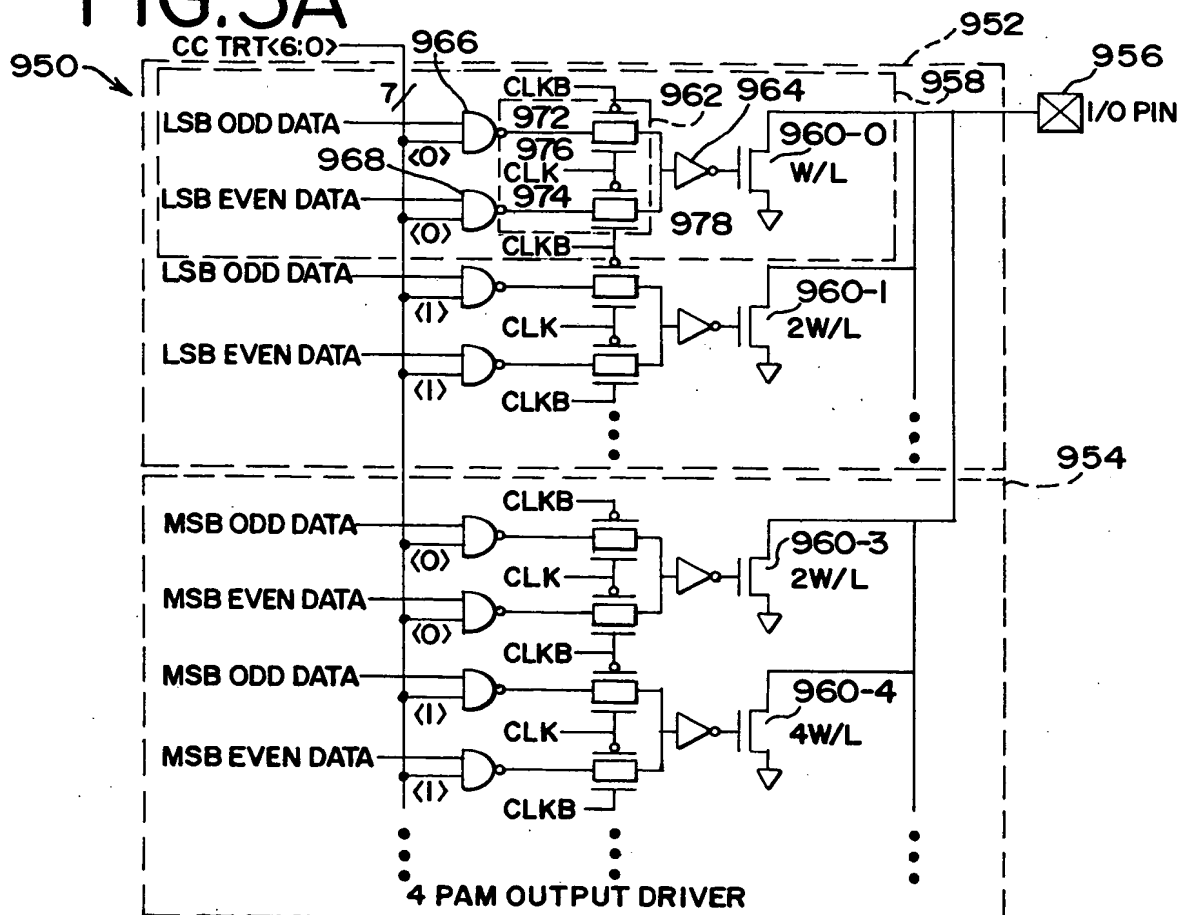


FIG. 3B

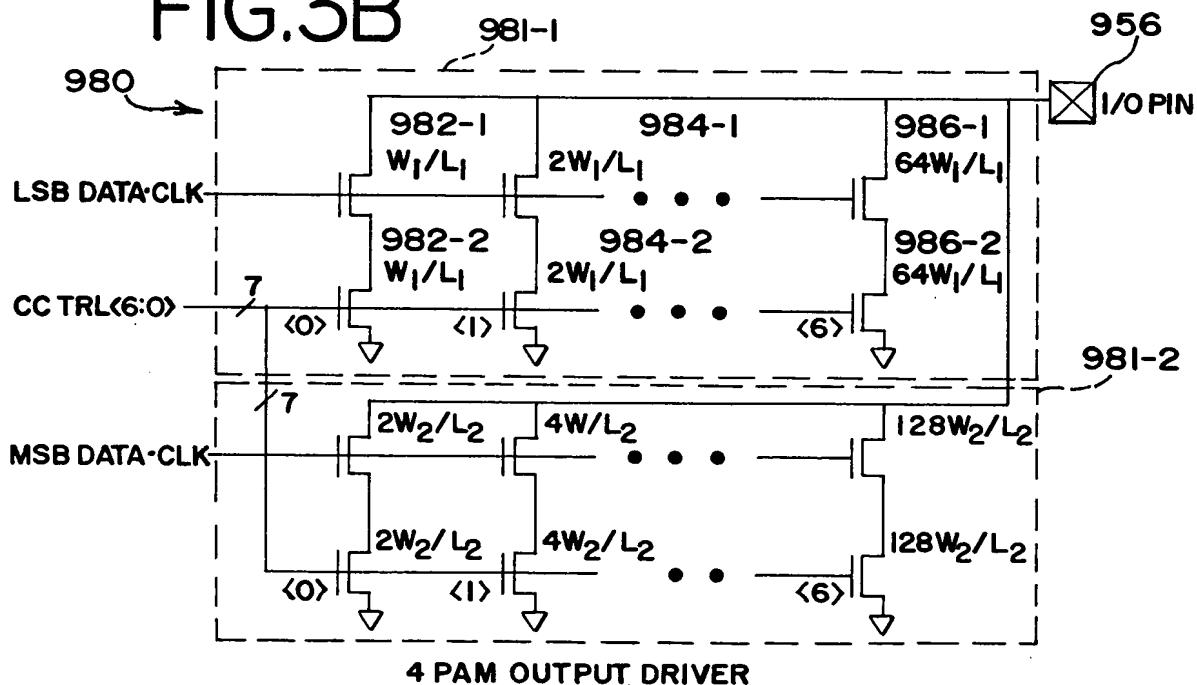


FIG. 4A

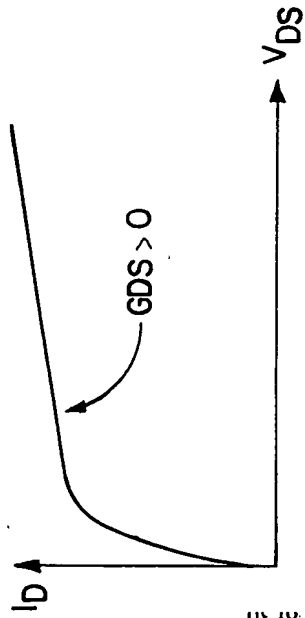


FIG. 4B

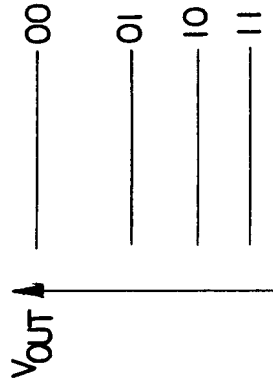


FIG. 4C

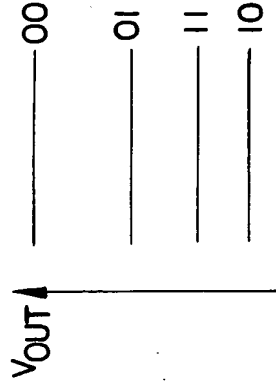


FIG.5A

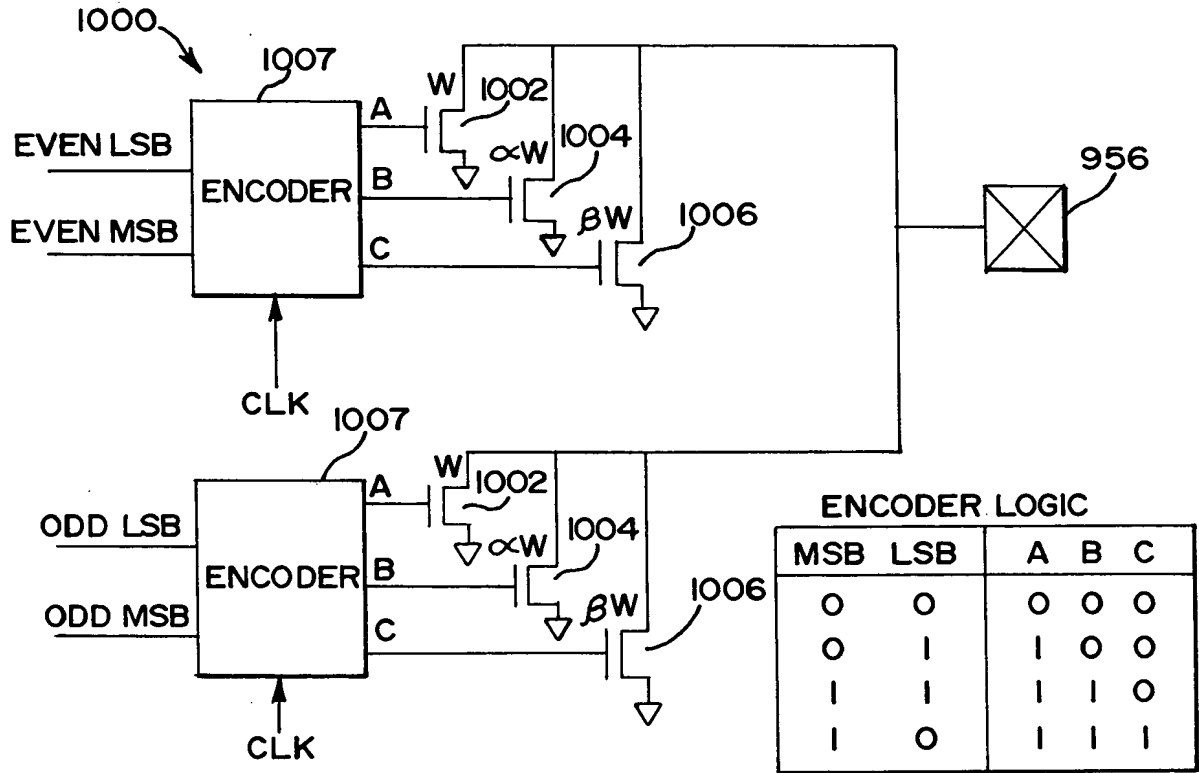


FIG.5B

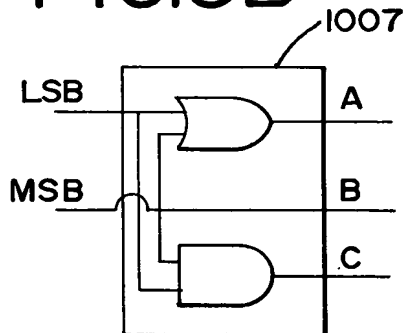


FIG.5C

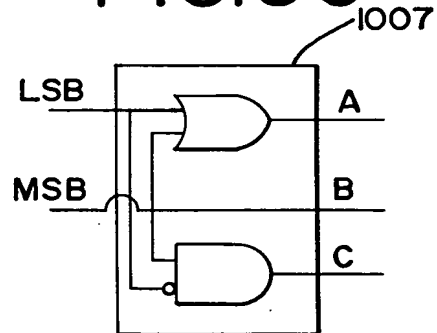
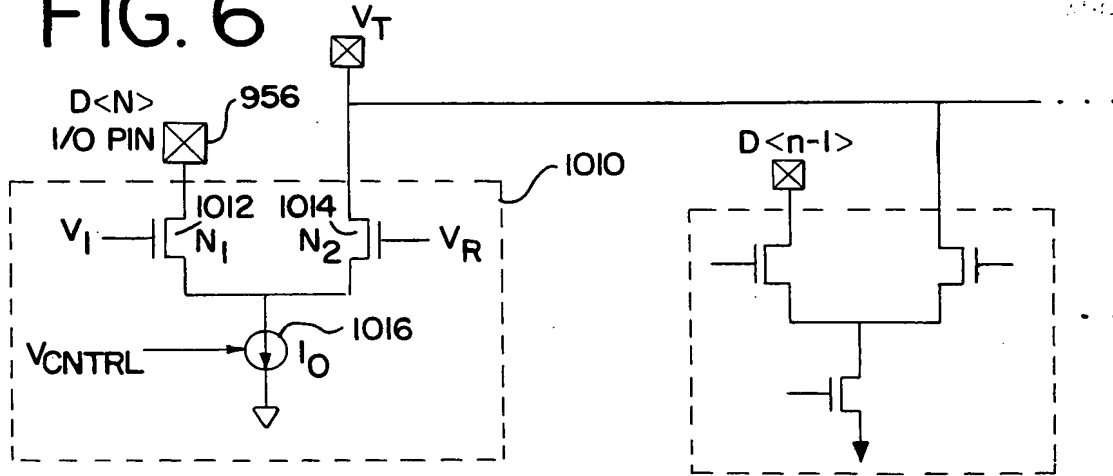


FIG. 6



CIRCUIT TO REDUCE SWITCHING NOISE

FIG. 7

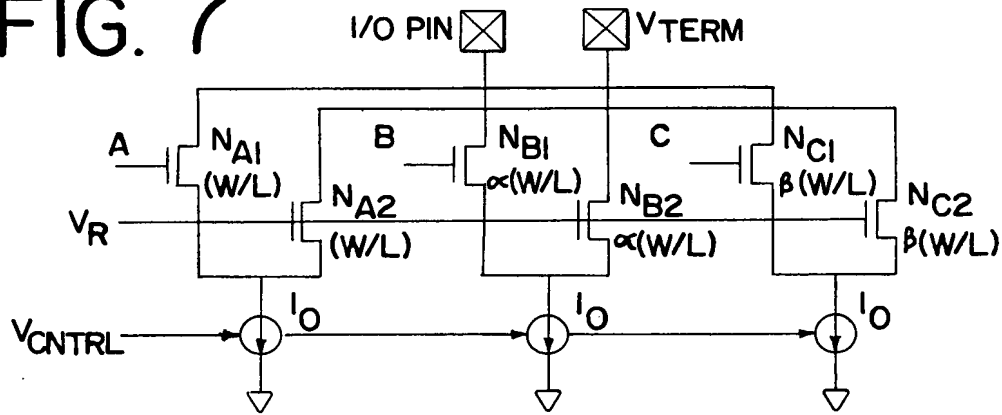
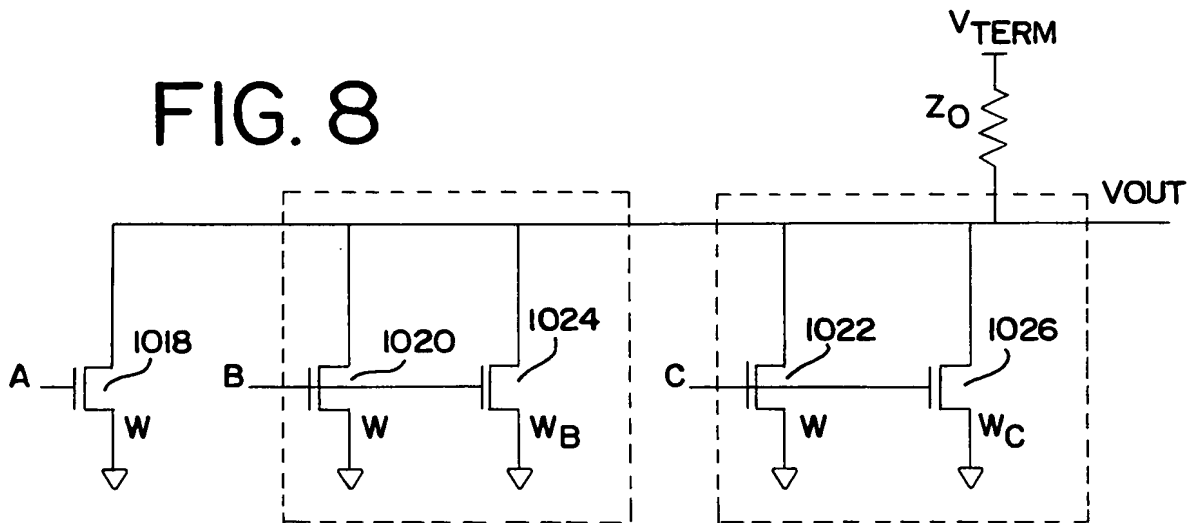


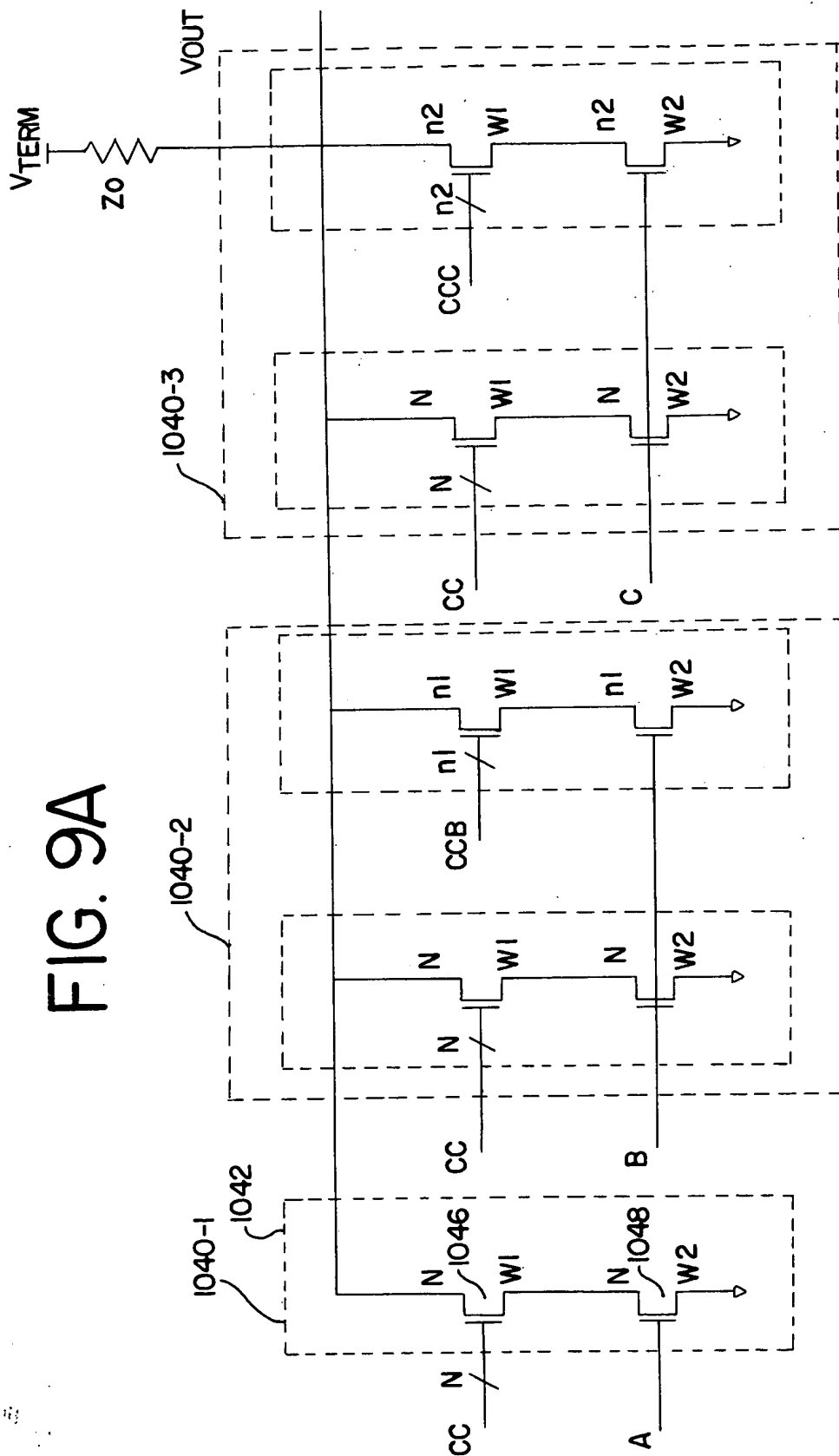
FIG. 8



GDS COMPENSATED MULTI-PAM OUTPUT DRIVER

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FIG. 9A



GDS COMPENSATED MULTI-PAM OUTPUT DRIVER WITH CURRENT CONTROL

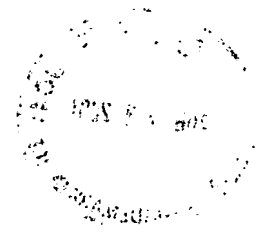


FIG. 9B

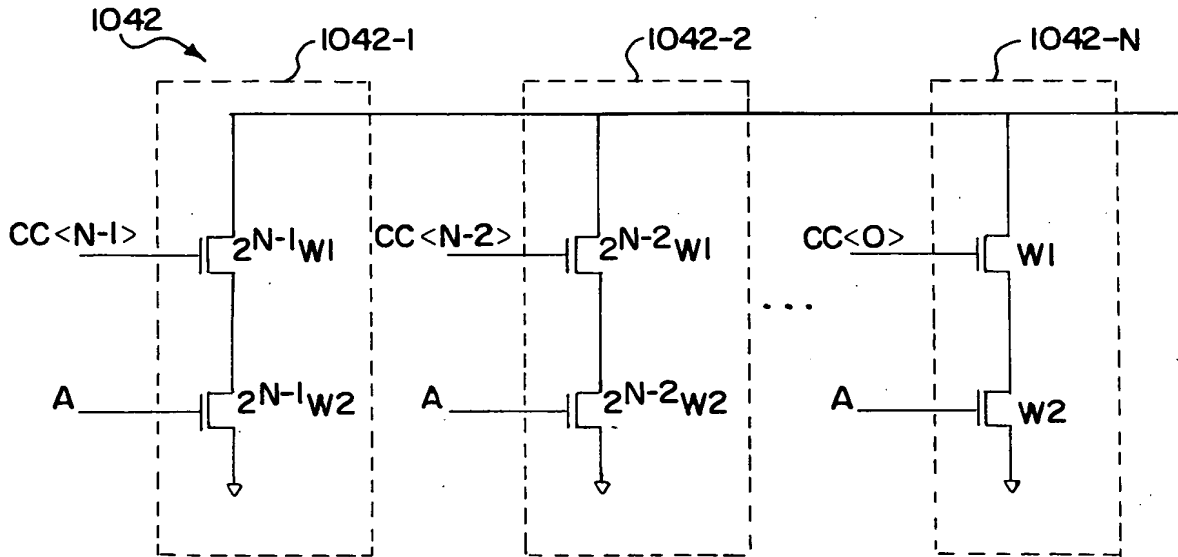
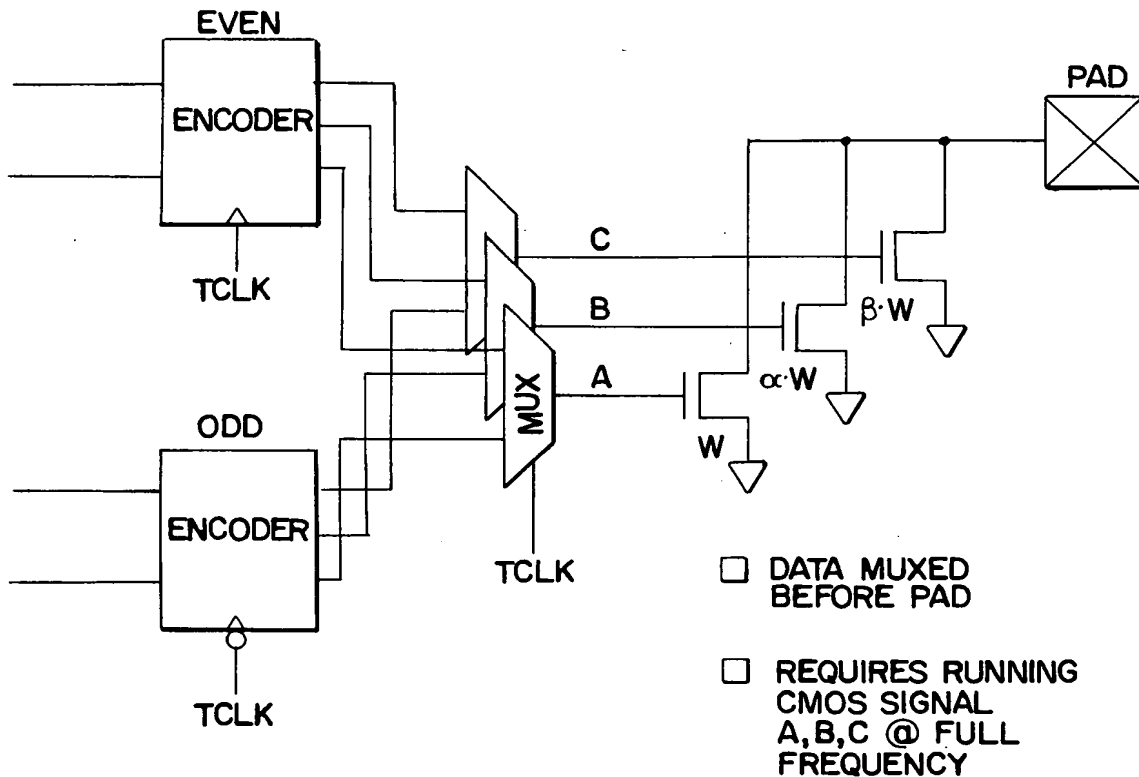


FIG. 9C



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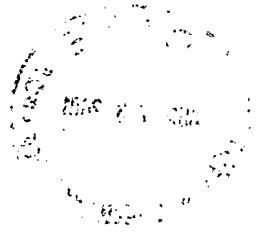
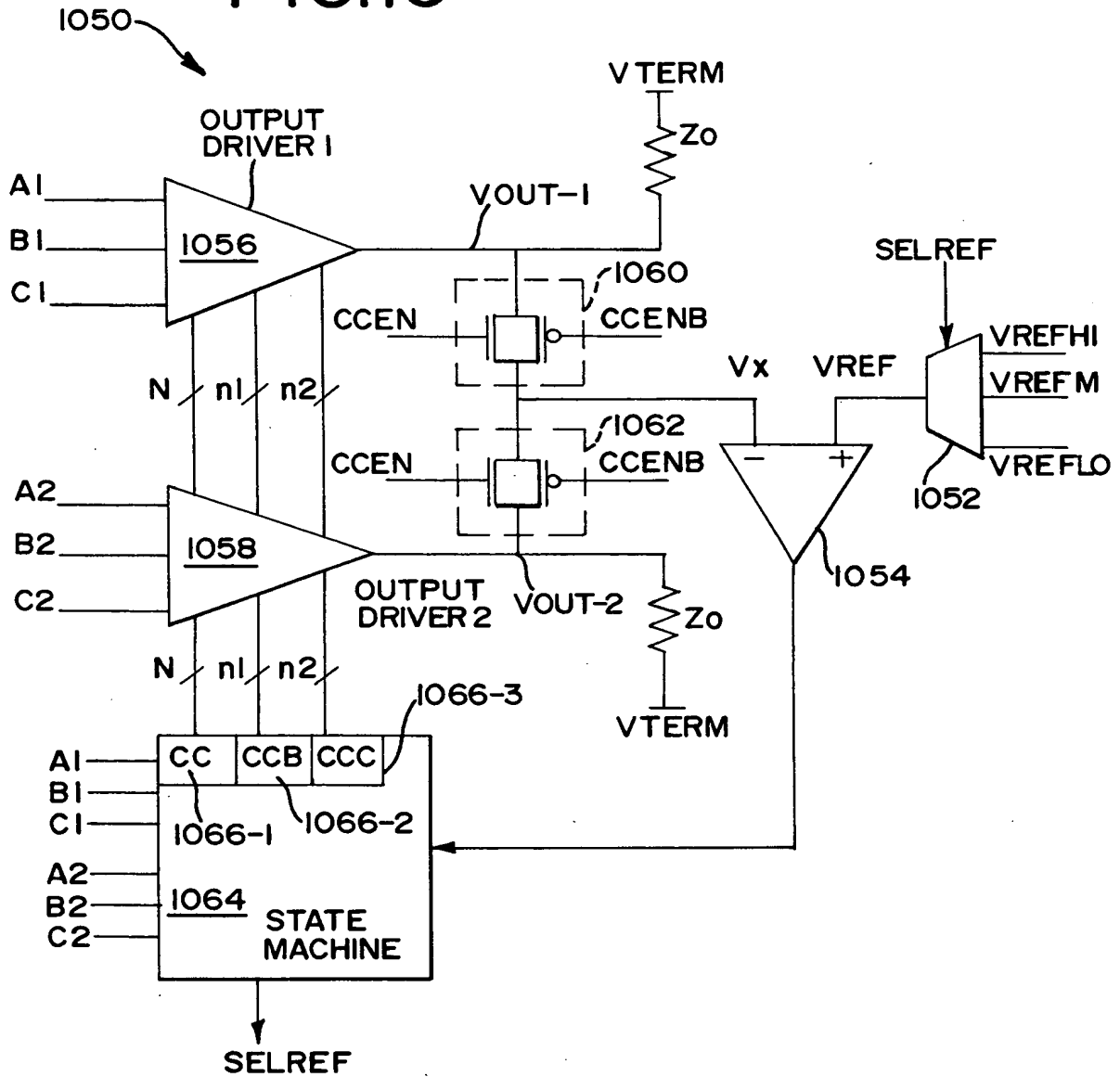


FIG.10



CIRCUIT FOR CALIBRATING THE GDS COMPENSATED
OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 11A

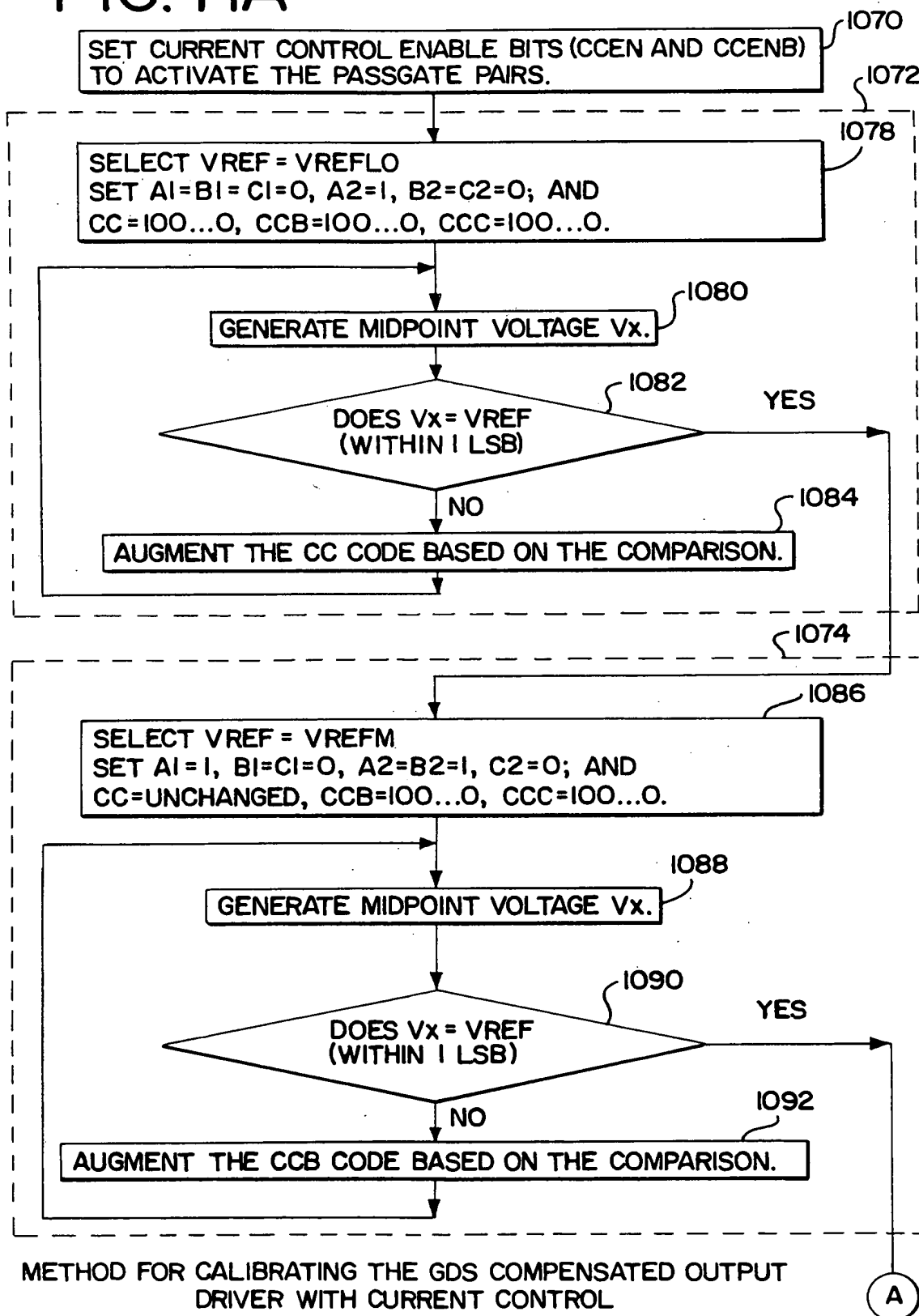
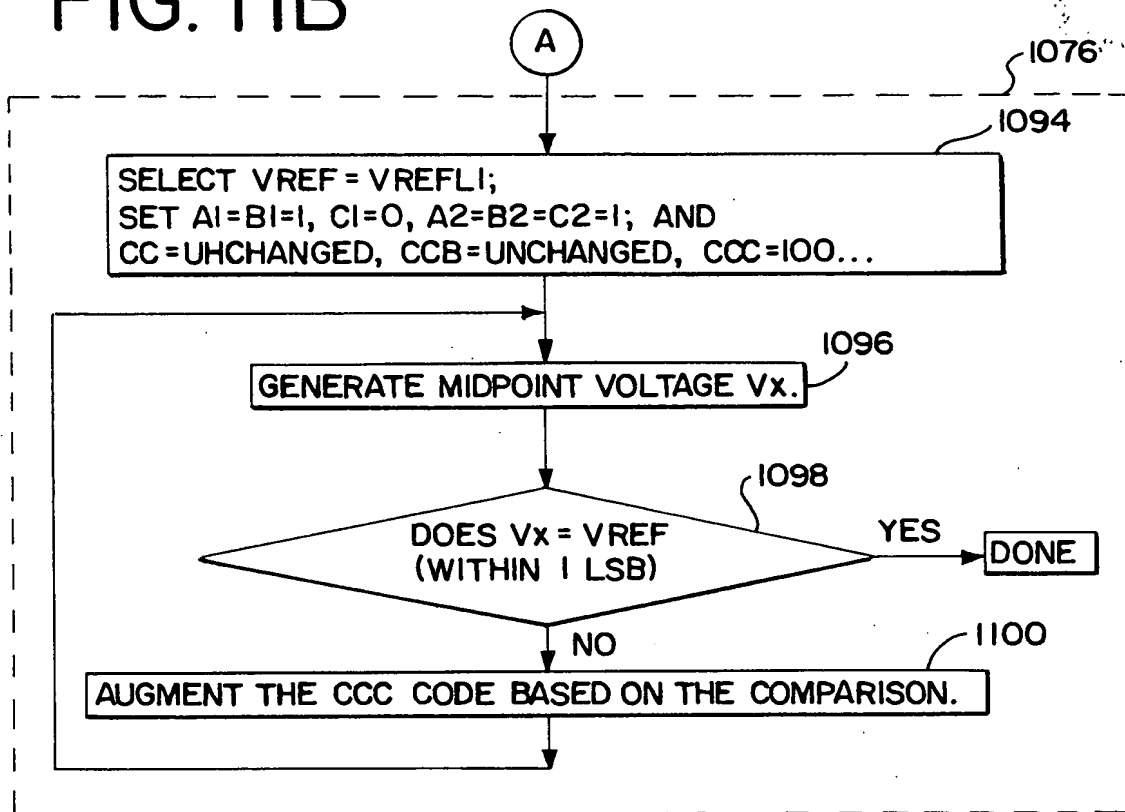
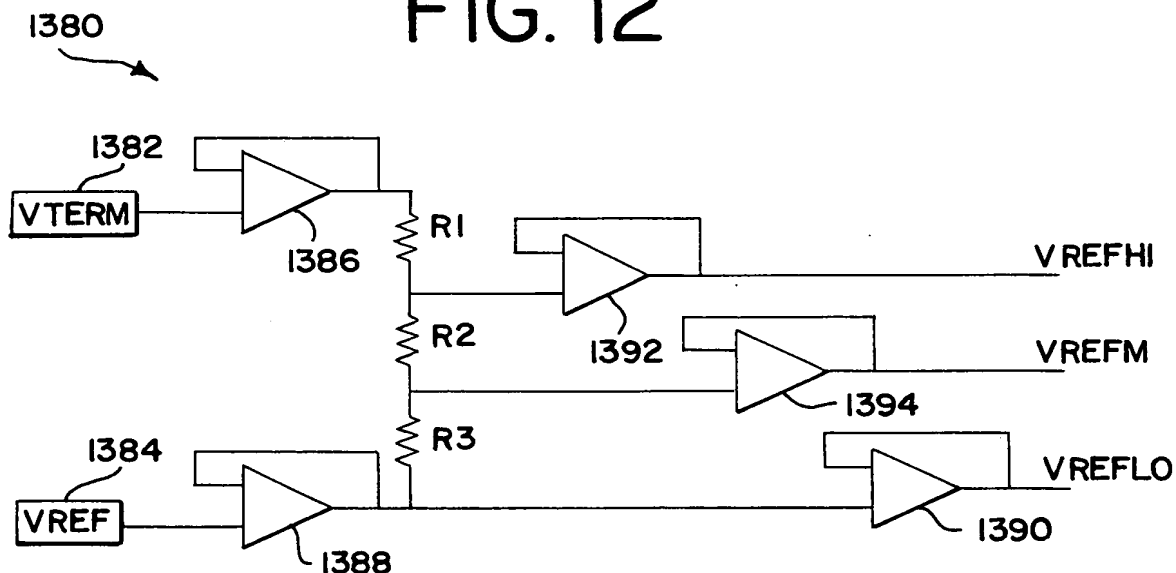


FIG. 11B



METHOD FOR CALIBRATING THE GDS COMPENSATED OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 12



[illegible]

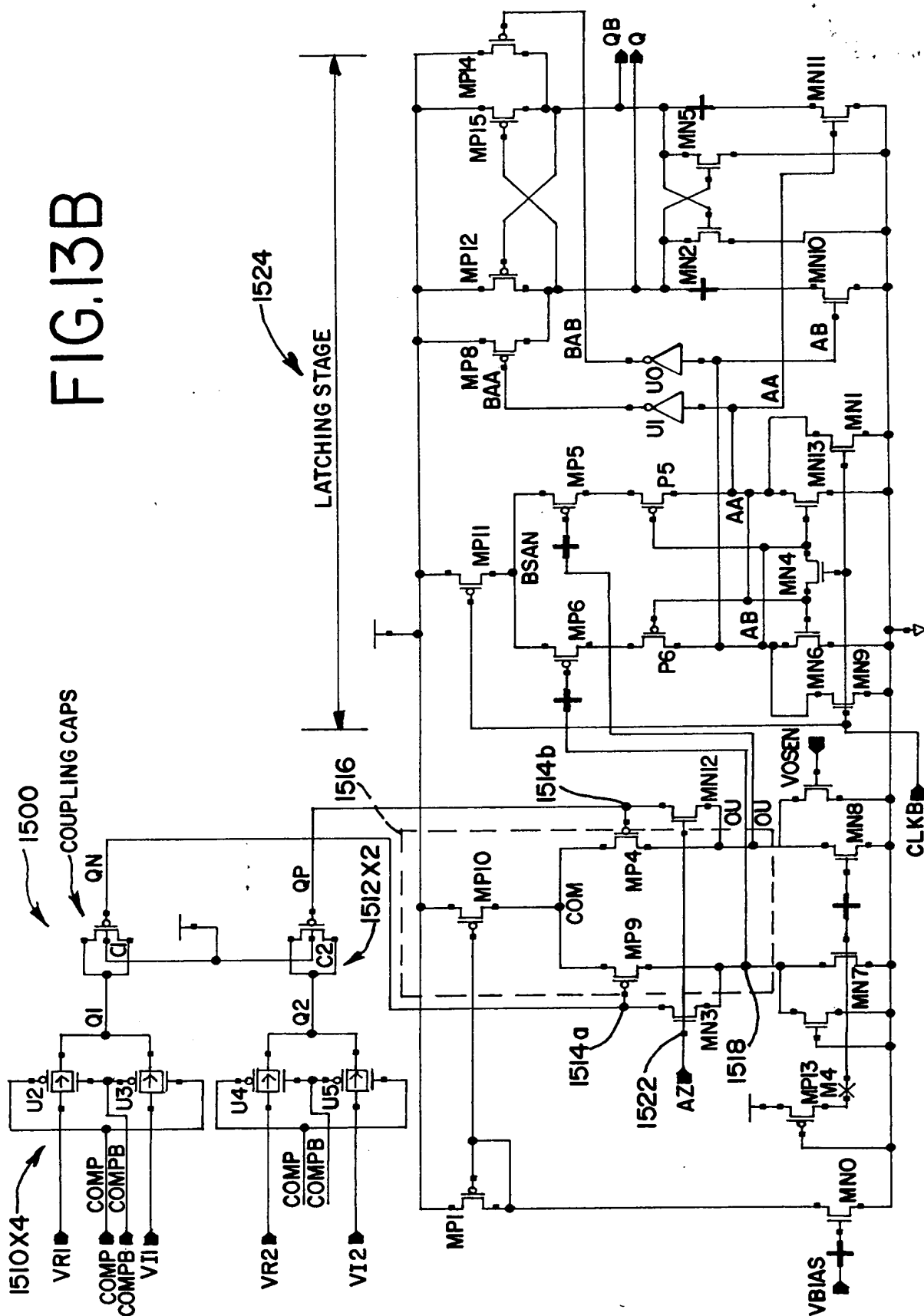
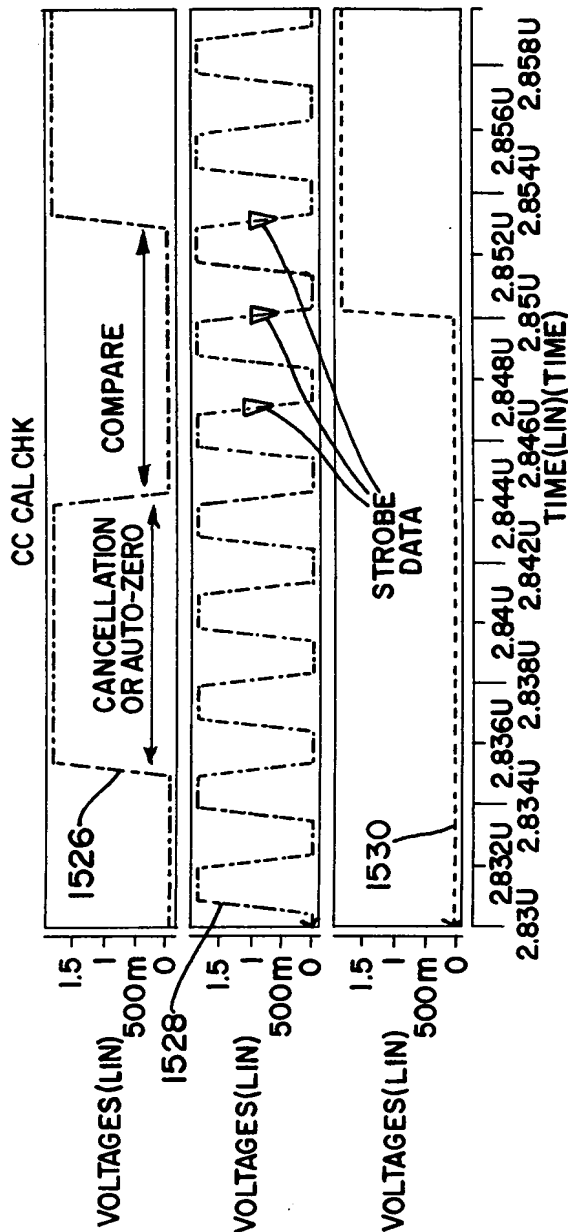
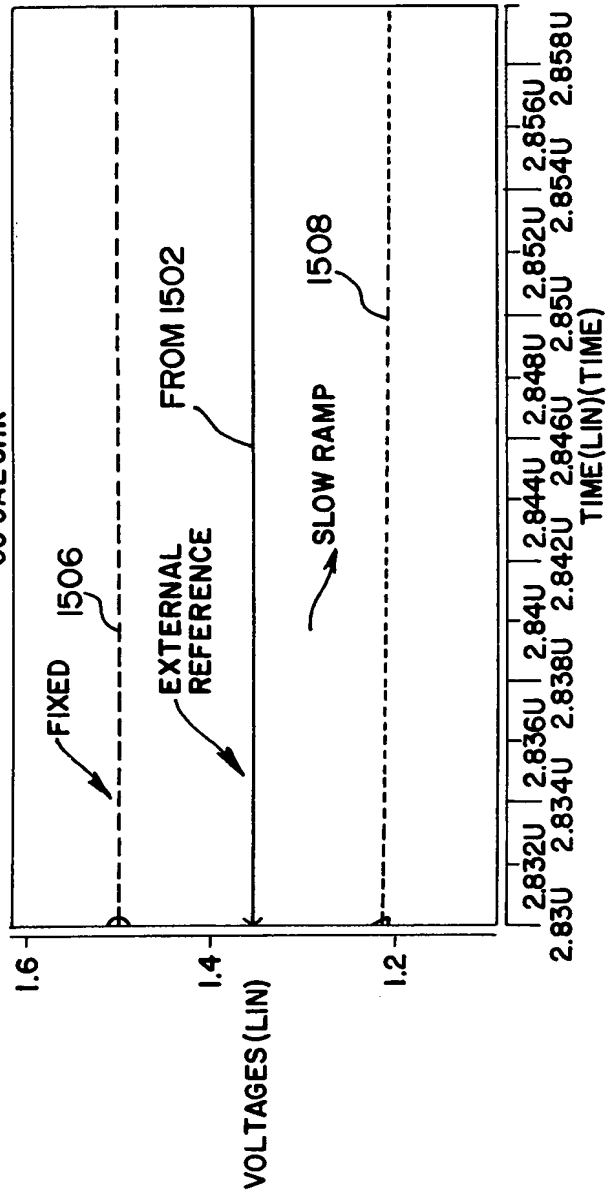


FIG. 13C

WAVE	SYMBOL
DO:AO:V(CC OUT)	---X---
DO:AO:V(DS)	---X---
DO:AO:V(AS)	---A---



CC CALCHK



WAVE	SYMBOL
DO:AO:V(vrefm)	---X---
DO:AO:V(inhi)	---O---
DO:AO:V(inlo)	---A---

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FIG. 13D

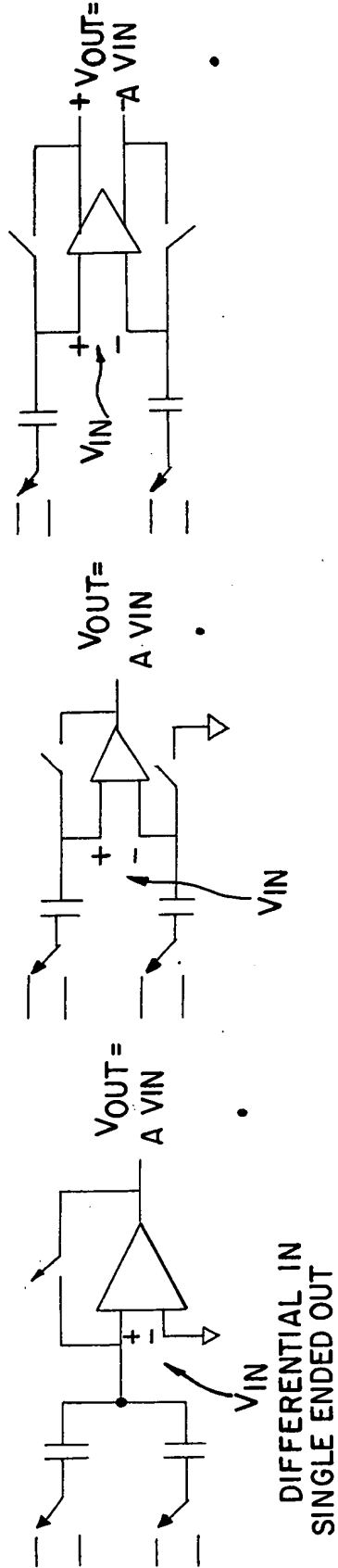
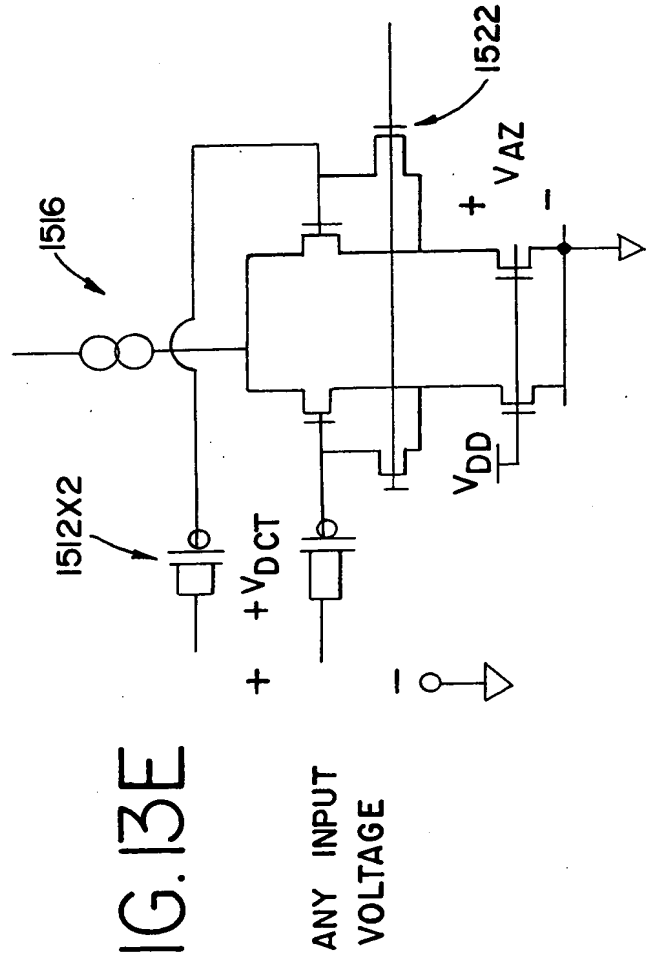
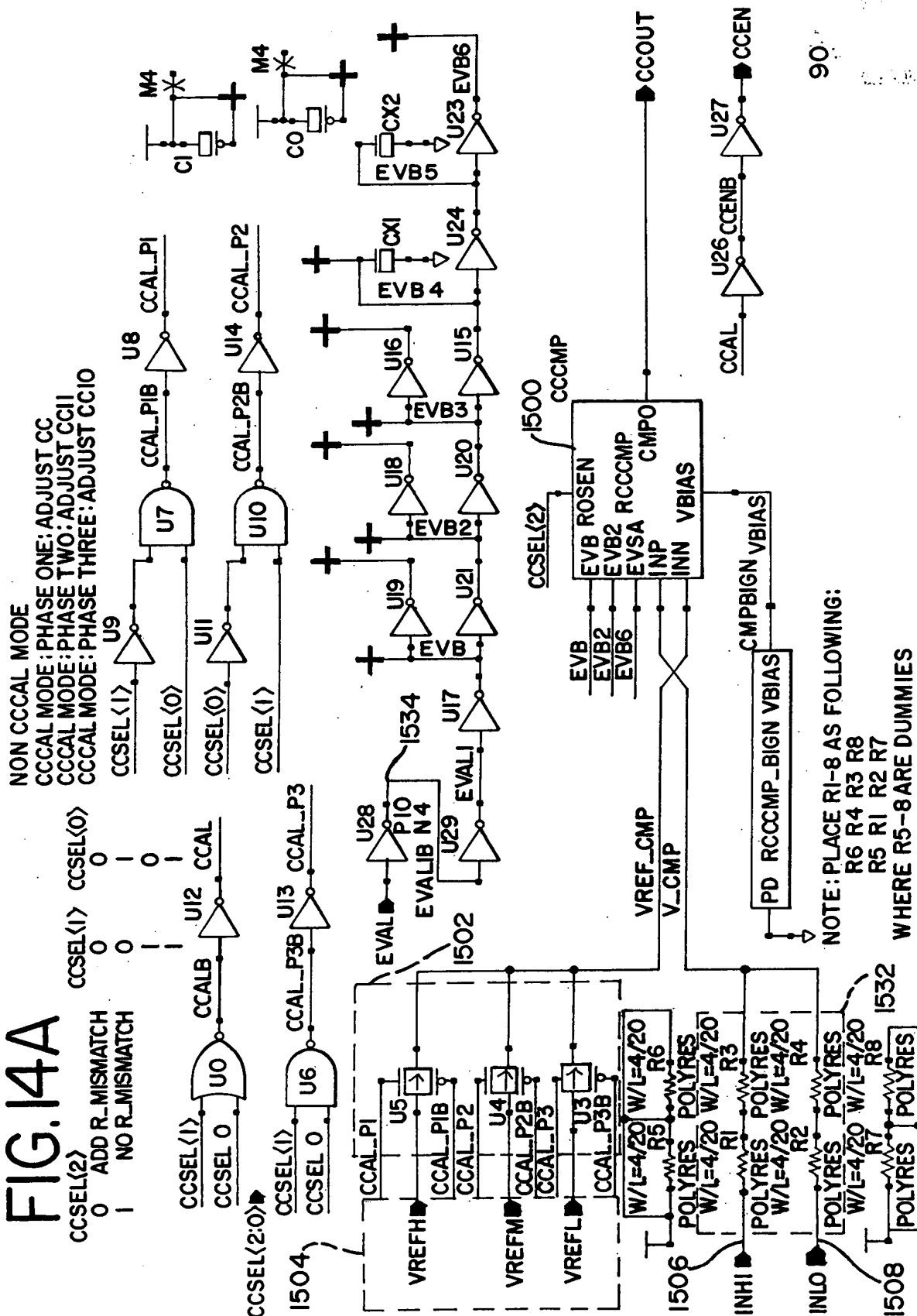


FIG. 13E



NON CCCAL MODE



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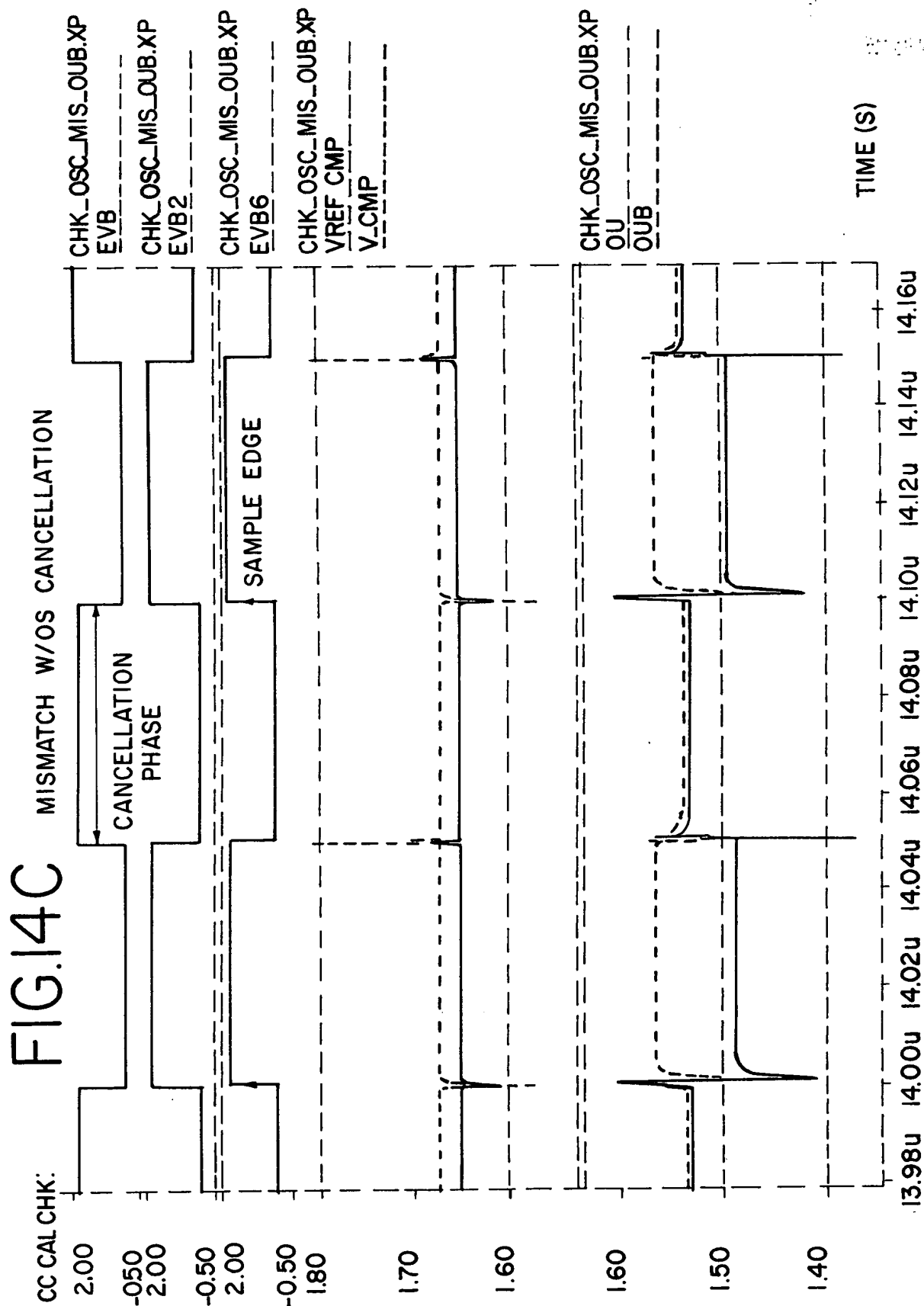


FIG. 14D

W/OS CANCEL

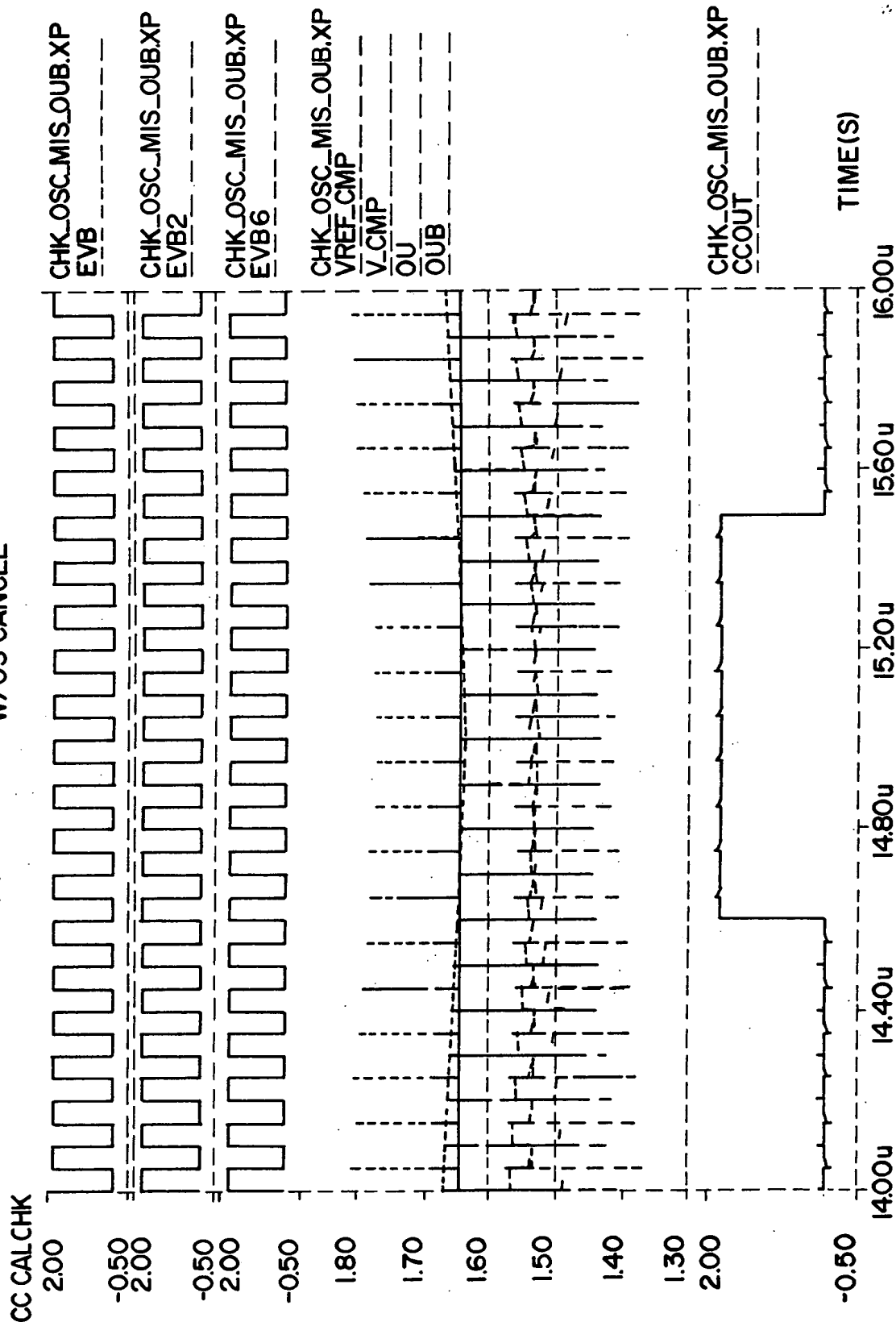


FIG.15A

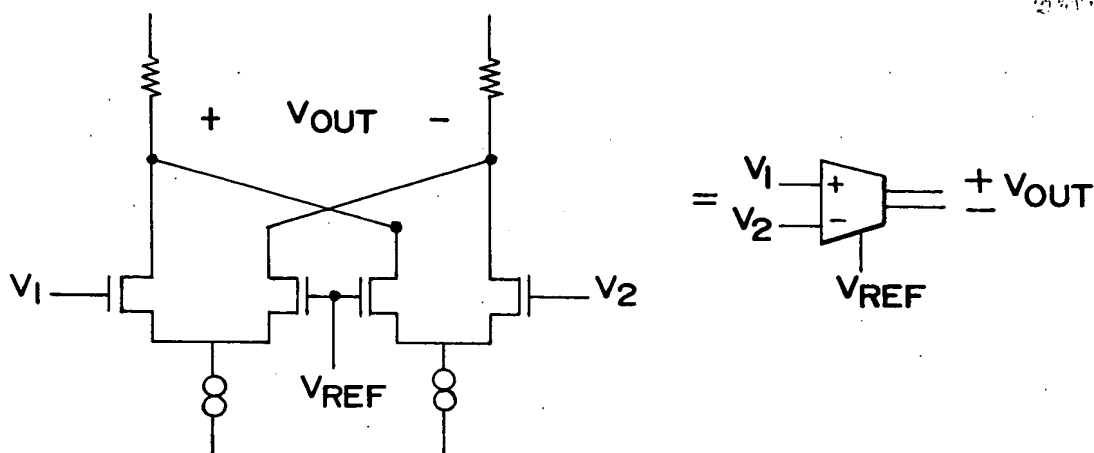


FIG.15B

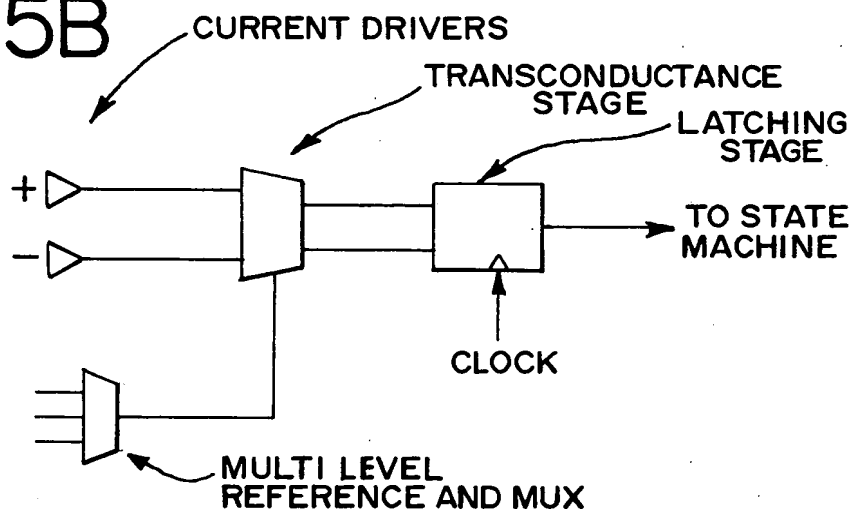


FIG.16

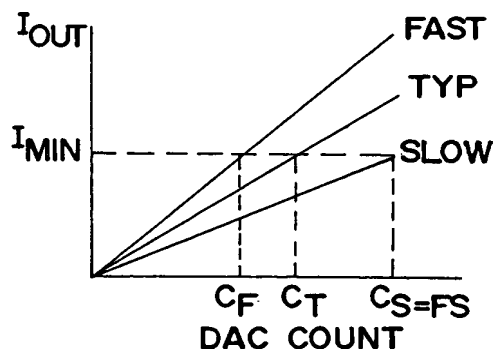
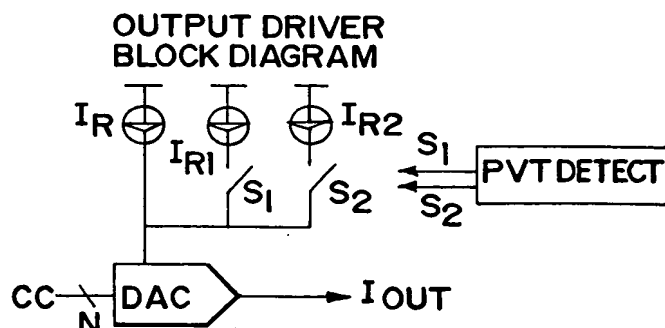


FIG.17



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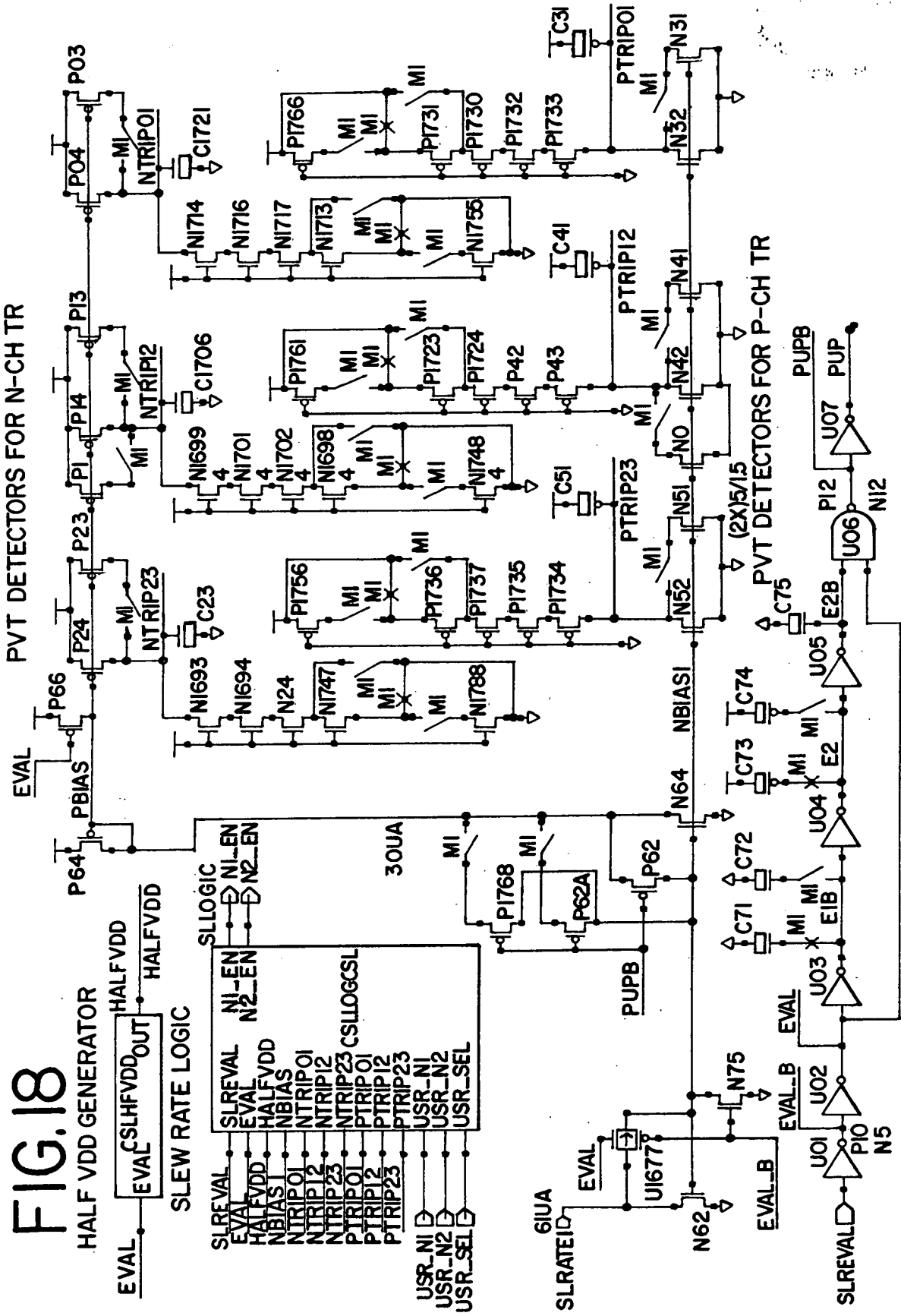


FIG. 19A

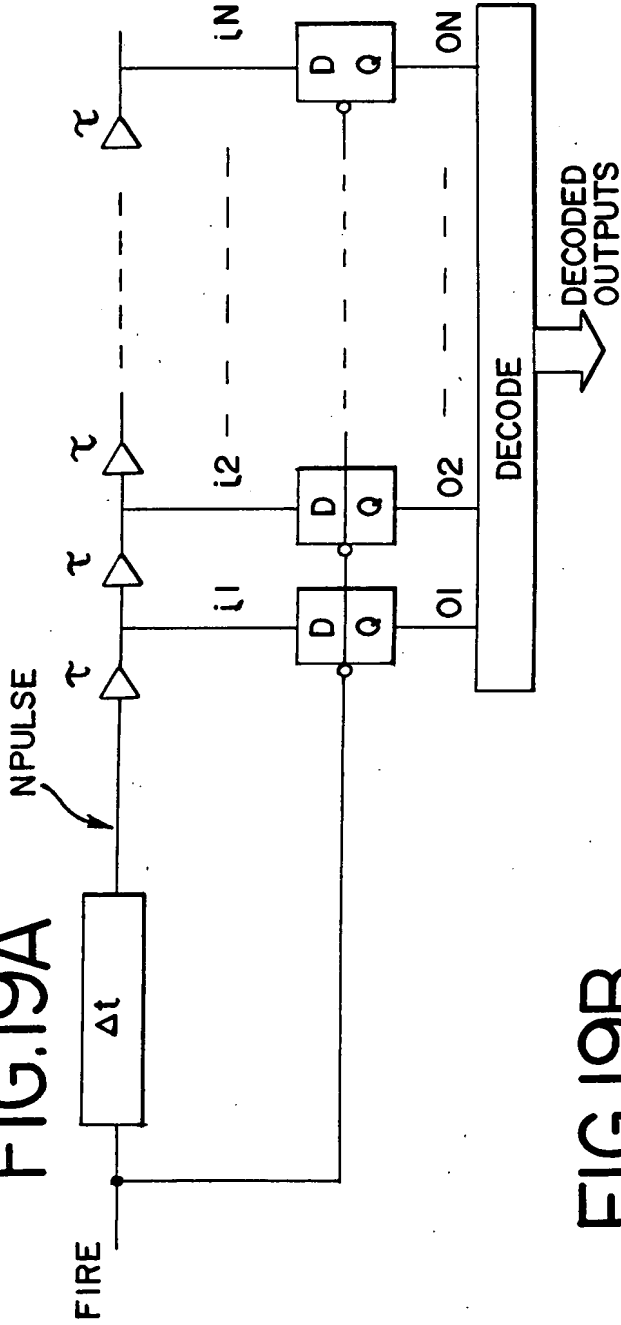


FIG. 19B

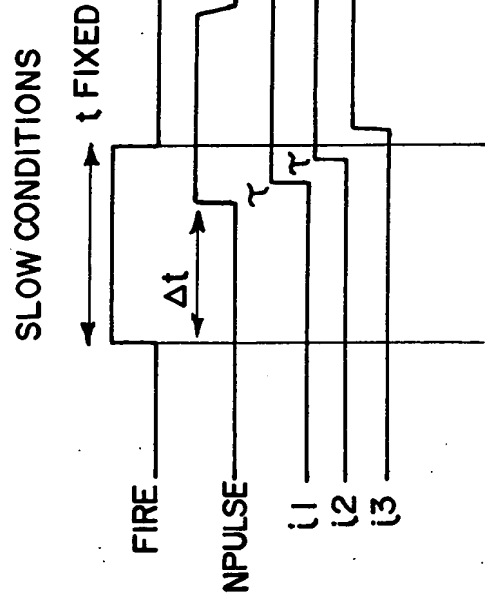


FIG. 19C

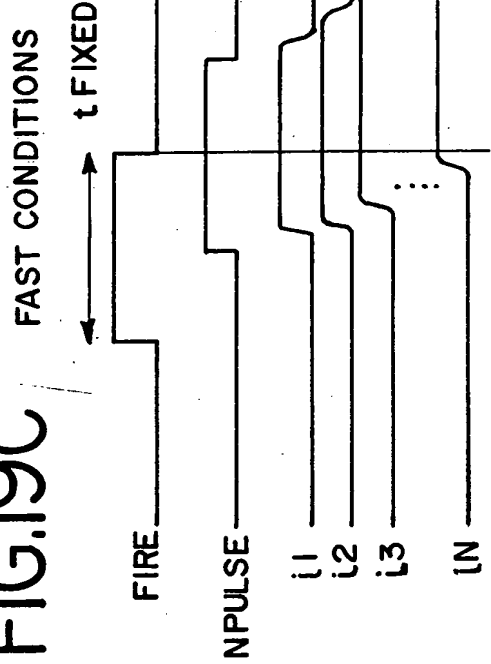
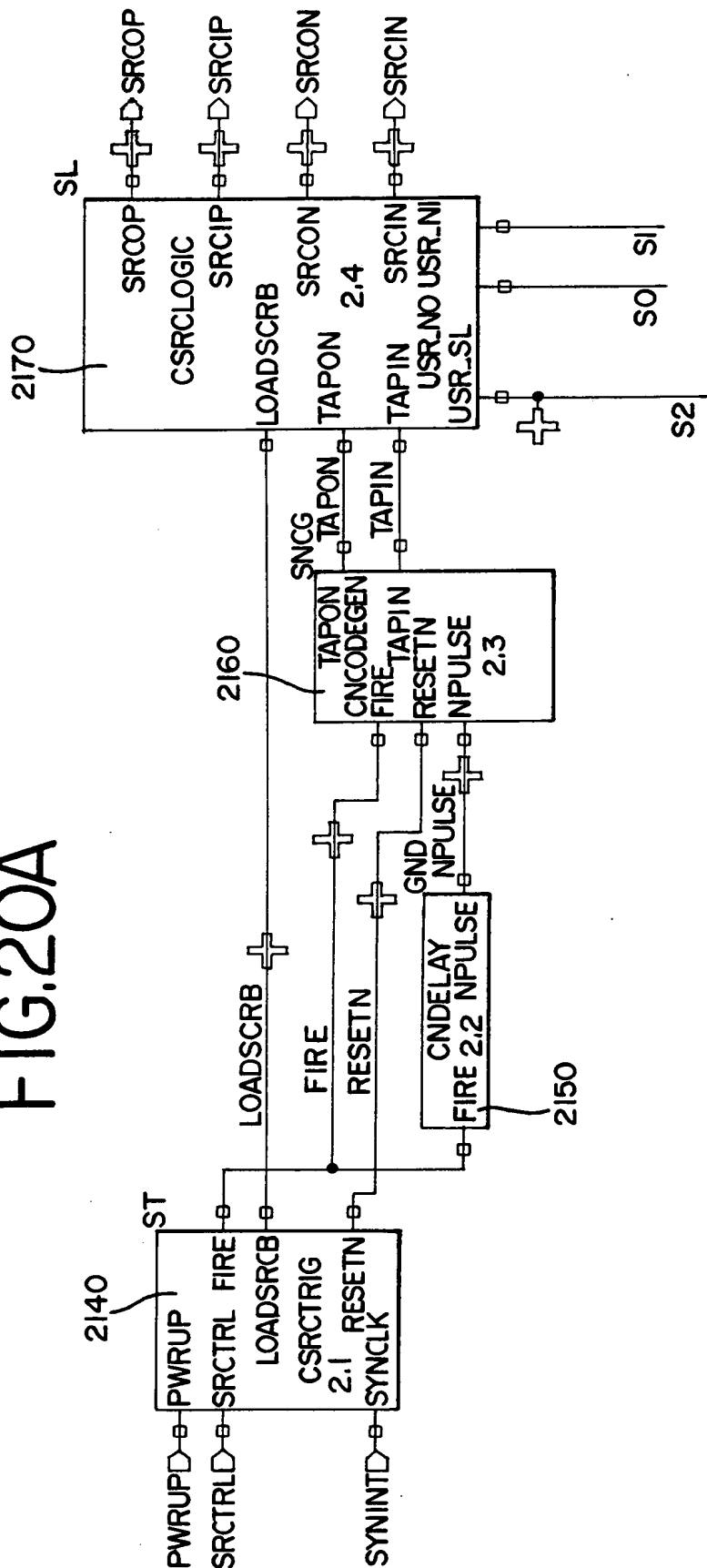
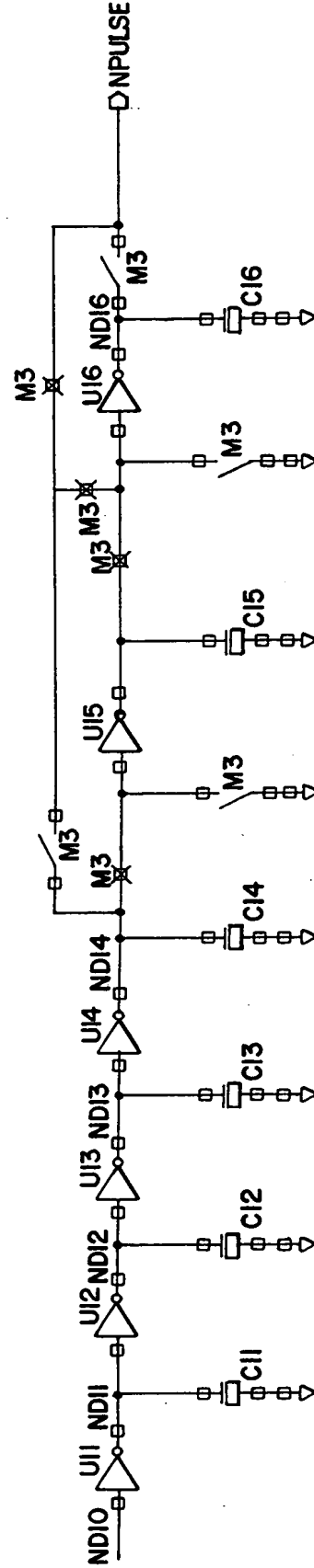
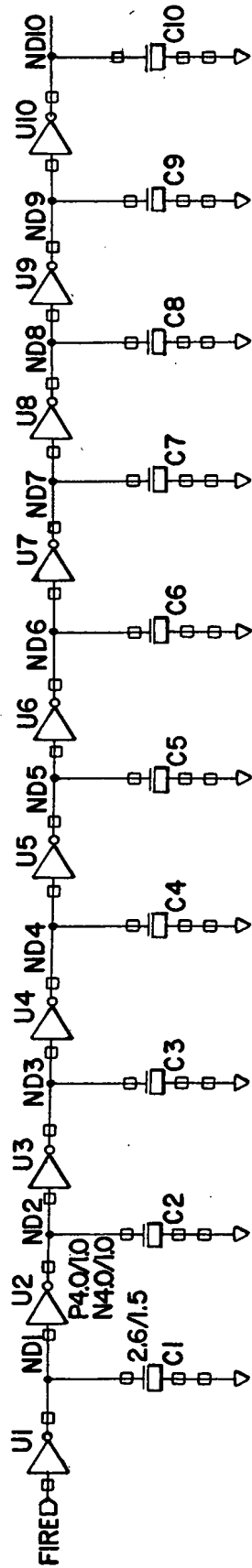


FIG. 20A



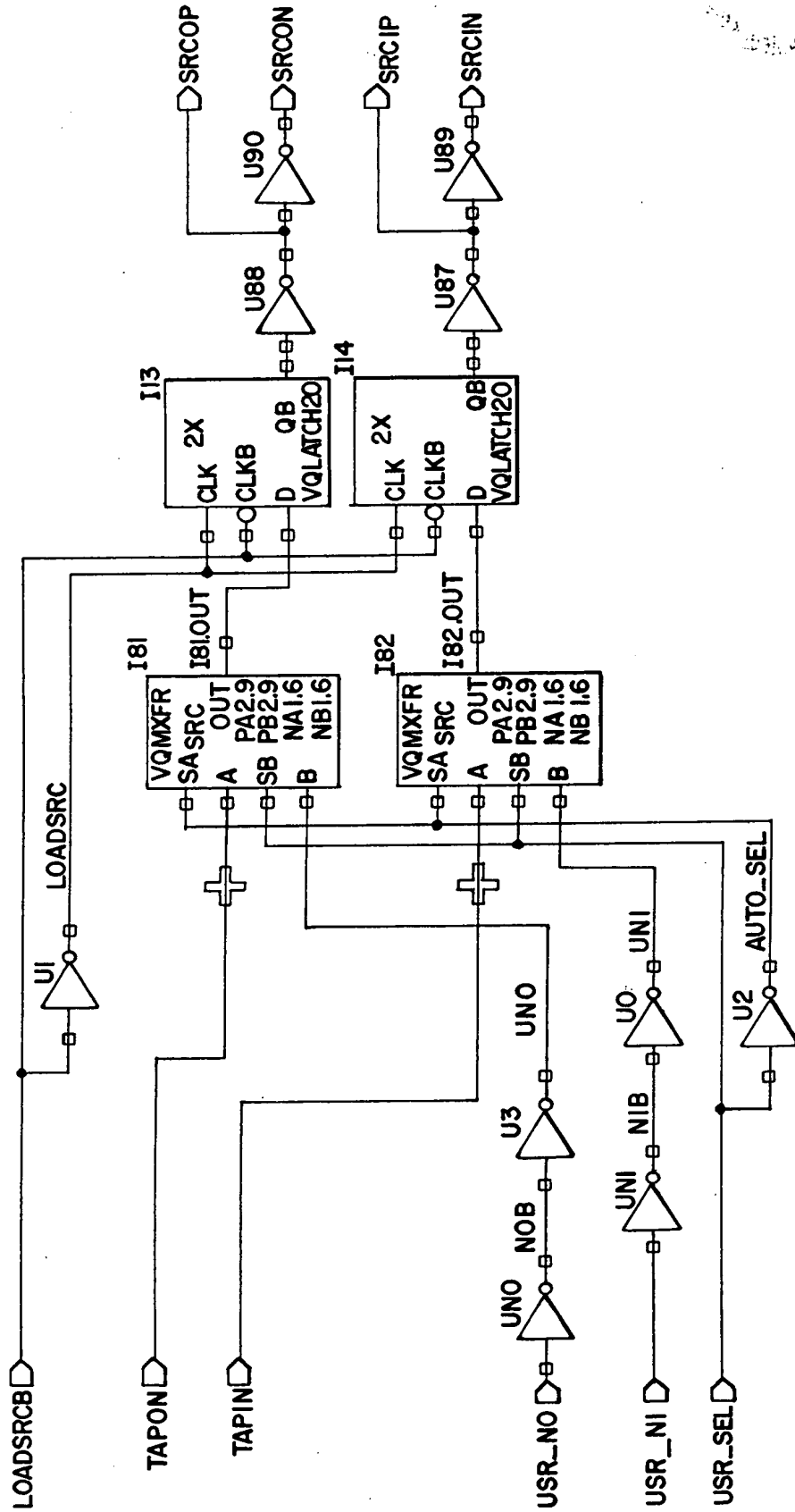
The diagram illustrates the control logic for the IIG.20B. It features a 258-bit shift register (U1) that provides a sequence of control signals. These signals are processed by a series of flip-flops (FF1 through FF6) and logic gates (U2 through U6) to generate the final control signals: SRCTRL, PWRUP, SYNCCLK, and LOADSRCB. The circuit also includes a 258-bit shift register (U2) and a 258-bit shift register (U3) for additional control signals. The output of the shift register is connected to the control inputs of the flip-flops and logic gates. The flip-flops are configured as D-type flip-flops with clock (CLK), data (D), and reset (RST) inputs. The logic gates are configured as AND and OR gates. The final control signals are generated by the output of the flip-flops and logic gates.

FIG.20C



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FIG.20E



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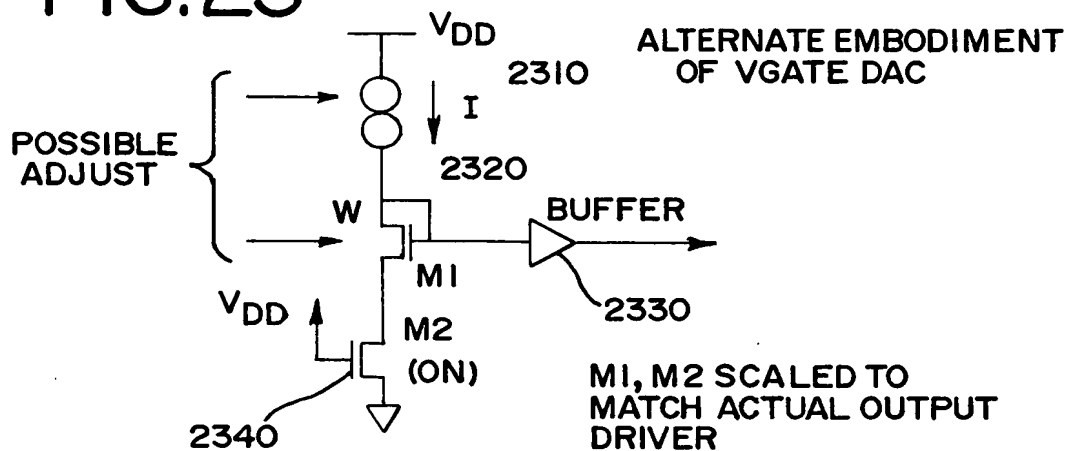
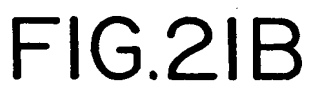
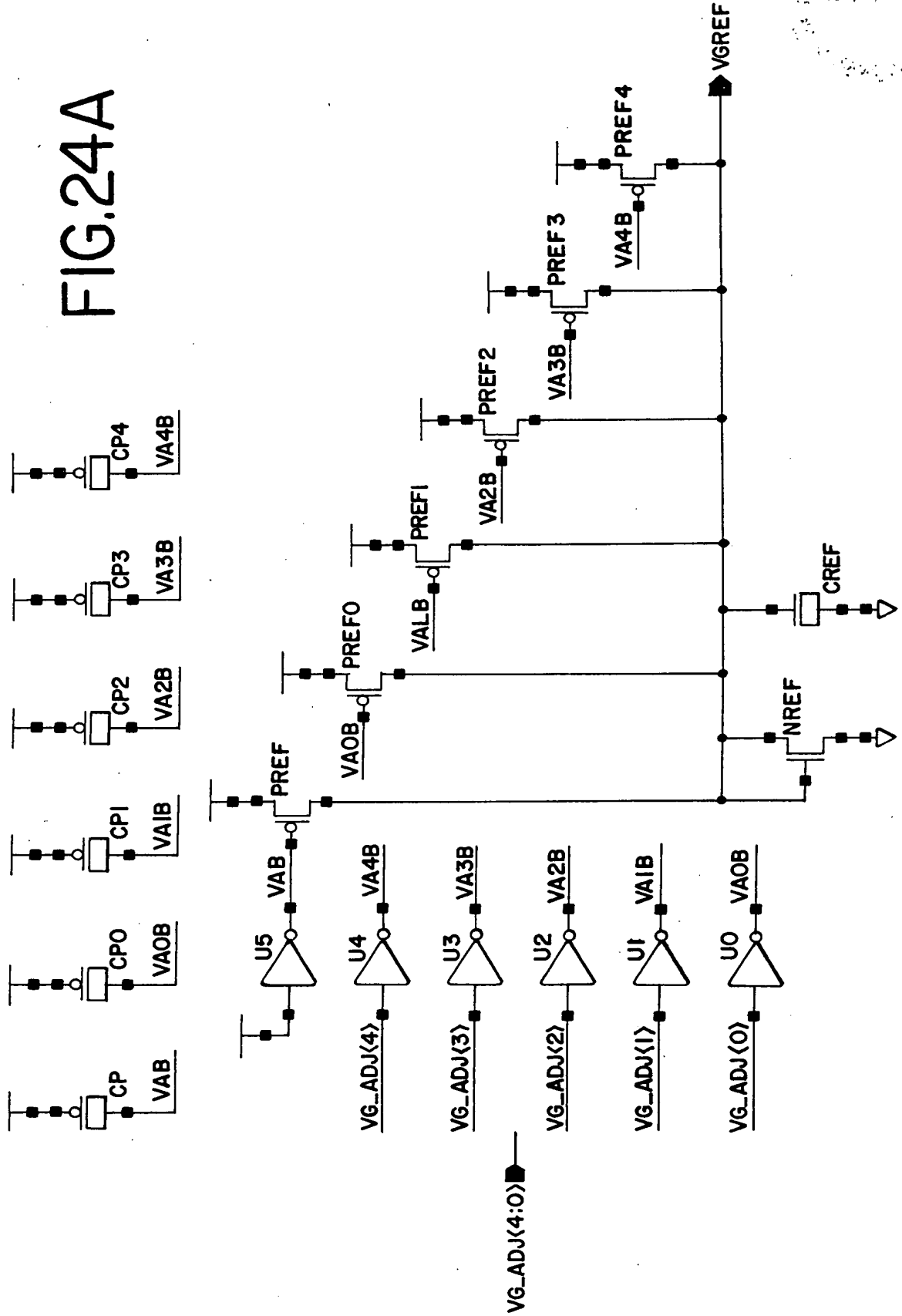


FIG. 24A



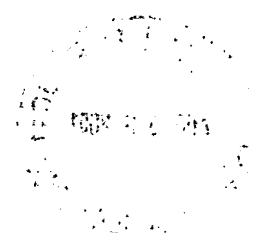


FIG.24B

